Pulse-doped GaAs MESFETs with planar self-aligned gate for MMIC

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Abstract

A pulse-doped GaAs MESFET with n+ self-aligned planar gate has been developed. This device shows excellent drain current linearity and minimum noise figures of 0.72dB (1.15dB) with associated gains of 10.5dB (8.5dB) at 12GHz (18GHz). Furthermore, excellent uniformity and reproducible device characteristics also have been realized.

Introduction

Direct satellite broadcasting, microwave communication and radar systems have been rapidly expanding to date. GaAs-based devices are very attractive to application for those systems because of their excellent high frequency, low noise and high power performances. Microwave monolithic integrated circuits (MMICs) have been expected as the key devices to improve performance and reliability and reduce size and cost of those systems.

High electron mobility transistors (HEMTs) have been recognized excellent low noise devices [1]-[5], but HEMTs have some disadvantages for MMIC applications.

<1> Most of HEMTs are fabricated on MBE grown materials which results low through-put and high cost.

<2> Most of HEMTs have recess gate structure which results poor uniformity and reproducibility of device characteristics because of lacking in the controllability of recess etching.

On the other hand, ion implanted technologies, which are widely used for high density digital circuits, have been recently refined for MMIC [6] [7]. Although they showed quite uniform device characteristics, the performance of their devices is not so high as those of HEMT s.

We have implemented a pulse-doped structure [8] as a GaAs MESFET channel ,which is very simple structure rather than HEMT, and planar gate structure based on self-aligned ion implantation for MMIC.

In this paper, we describe a process technology of our pulse-doped GaAs MESFET and their excellent microwave performance. In addition, excellent uniformity and reproducibility of device characteristics are also shown.

Pulse-doped structure

As shown in Fig.1, a pulse-doped structure was implemented as a MESFET channel to obtain high transconductance, low gate leakage current,and good linearity of drain current with gate bias.

An undoped p- GaAs buffer layer (1μm), Si doped GaAs active layer ($4x10^{18}/cm^3$,100Å),and undoped n- GaAs cap layer (300Å) are successively grown by OMVPE on a semi-insulating GaAs substrate. An undoped p- and n- layer are formed by controlling V/Ⅲ ratio of source materials.

Trimethyl gallium (TMG) and arsine (AsH_3) are used to grow GaAs, and disilane (Si_2H_6) is used as the n-type dopant. An extremely abrupt change in carrier profile and quite uniform epilayer were obtained by using specially designed OMVPE systems. The uniformity of thickness and carrier concentration of epilayer were less than 3% over a 2″ φ wafer.

Electron mobility of pulse-doped structure is about $1900cm^2/V\cdot s$ at R.T. We also observed the quantum well formation of this structure. Detailed analysis will be reported elsewhere.

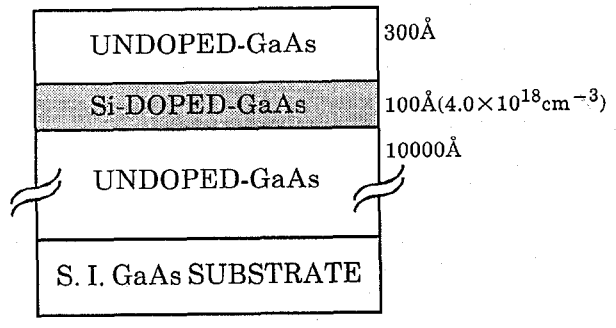

Fig.1 Epitaxial layer structure of pulse-doped GaAs MESFET

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Threshold voltage (Vth) for pulse-doped MESFET under the fully depleted layer approximation is given by

$$Vth=\phi B-(qN_2/2\varepsilon s)X_2^2-(qN_2/\varepsilon s)X_1X_2-(qN_1/2\varepsilon s)X_1^2 \quad (1)$$

where ϕ_B is the shottky barrier height, q is the electron charge, N_1, X_1 are donor density and thickness for cap layer, respectively, N_2,X_2 are those for a channel layer and εs is permittivity for semiconductor. According to equation (1), Vth of this pulse-doped MESFET was calculated to be -1.0V.

Device fabrication

Planar process is necessary to improve uniformity and reproducibility of device characteristics which are most important for MMIC applications.

Our process was based on T-shaped dummy gate self-alignment like a SAINT [9] ,which allow that n+ region was formed self-alignely for gate region and subhalf micron gate can be formed by using a conventional optical lithography. Fabrication processing sequence is briefly as follows.

First, multiple layers shown in Fig.1 are grown by OMVPE. Then active areas were isolated by mesa etching. T-shaped resist mask with 0.2μm undercut amount was formed by anisotropic RIE. Si ions were implanted for n+ layer formation with $6\times10^{13}/cm^2$ dose at 90KeV through SiN film.

Rapid thermal annealing (RTA) was used for activation annealing of the ion implanted layers. Details for annealing process are mentioned later. Source and drain ohmic contact were formed by evaporating Ni/AuGe and successively alloyed at 450 °C. Finally, gate metal which consist of Ti/Pt/Au was substituted to the dummy gate. Fig.2 shows a cross-section of fabricated FET. The gate metal was overlapped the insulator to reduce the gate resistance and keep alignment requirements. The gate length is 0.3μm ,gate metal length is 1.0μm and source/drain electrode spacing is 4.0μm.

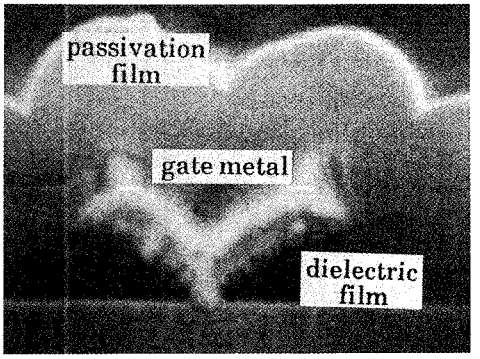

Fig.2 Cross section SEM photograph of a fabricated MESFET

RTA is a promising technique to activate implanted ion because RTA is effective in achieving high activation efficiency without significant impurity diffusion. Annealing condition was optimized in order to maintain the abrupt change in the carrier profile of pulse-doped structure and reduce source resistance. Fig.3 shows electron profiles after RTA, which are deduced from capacitance-voltage (C-V) measurement. It can be seen that the higher annealing temperature, the more the abruptness of carrier profile were degraded. The degraded pulse-doped structure cause the poor pinch-off characteristics. Although, lower temperature annealing cause to increase sheet resistance of implanted region resulting increase source resistance, the sheet resistance of implanted region saturated above 860°C . Taking those results into account, the annealing condition was optimized to be 860°C for 2sec. Then the sheet resistance of the n+ region was 160Ω / □.

Fig.4 (a) and (b) show I-V characteristics for 0.3μm FET after RTA at 900 °C for 5sec and at 860 °C for 2sec, respectively. As the annealing condition was optimized, FET characteristics were improved at near pinch-off region, which is very important for low noise performance.

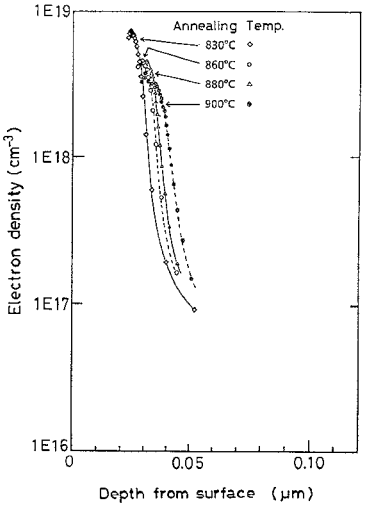

Fig.3
Electron profile deduced from the C-V measurement after RTA. (Annealing time is 5 sec.)

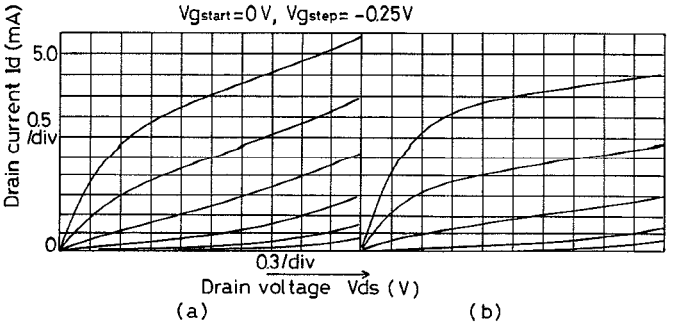

Fig.4 I-V characteristic of a 0.3μm FET after RTA at (a) 900°C for 5 sec and (b) 860°C for 2 sec.

DC characteristics

Fig.5 shows transconductance and drain current versus gate voltage of 0.3μm FET. Maximum transconductance is 360mS/mm,in addition transconductance shows a broad plateau with gate bias due to the excellent carrier confinement in the pulse-doped channel. Source resistance is 0.8Ω·mm, so the intrinsic transconductance is 505mS/mm. Shottky barrier height is 0.68eV and ideal factor is 1.20. The Vth is about -1.0V which is good agreement with the calculated value. The Vth changed by only 200mV as gate length goes from 1.0μm to 0.3μm. These results show that the short channel effect is suppress due to the pulse-doped channel. The standard deviation of threshold voltage is less than 100mV with -1.0V average value for 0.3 μm FET over a 2″ φ wafer[10]. In addition, quite reproducibility of Vth can be obtained as shown in Fig.6. The Vth for the wafers from different lots is consistently -1.0V with a standard deviation as low as 10%. These results could be obtained by using well established OMVPE technique, a simple pulse-doped structure and planar self-aligned gate process.

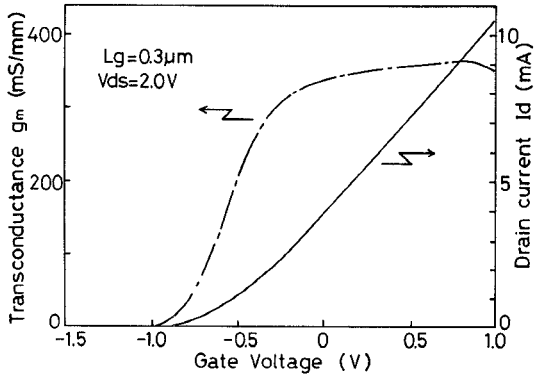

Fig.5 Transconductance and drain current versus gate voltage for a 0.3μm FET.

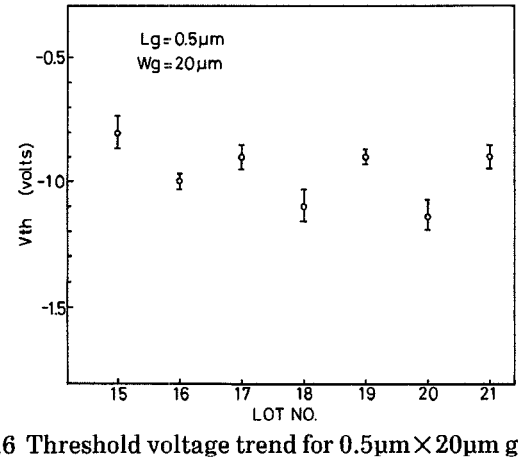

Fig.6 Threshold voltage trend for 0.5μm×20μm gate FET. ○ means average value over a 2″ φ wafer.
I means standard deviation over a 2″ φ wafer.

Microwave characteristics

S-parameter was measured by using Cascade Microtech probes and HP-8510B network analyzer. The current gain cut-off frequency f_T is as high as 40GHz which is obtained by extrapolating h21 with a -6dB/ oct slope. Fig.7 shows the f_T dependence of drain current. It can be seen that f_T shows a broad plateau with drain current. These characteristics are suitable for power and mixer IC applications. Even at low noise condition (=0.2Idss), f_T is over 30GHz. Fig.8 shows the equivalent circuit at low noise condition of 0.3μm×280μm FET, which is deduced S-parameter measurements. gm is 65mS (=232mS/mm), Rs and Rg is enough small for low noise device.

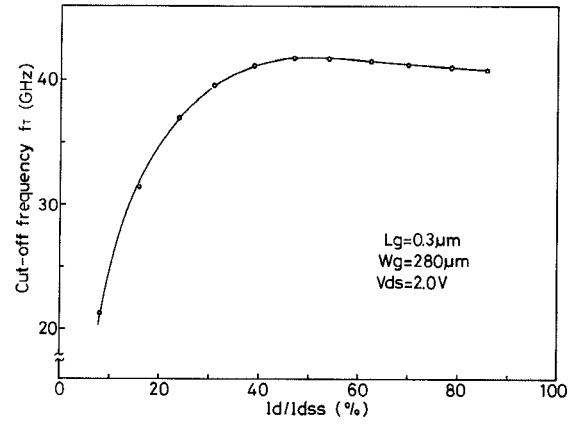

Fig.7 Cut-off frequency f_T as a function of drain current for a 0.3μm FET.

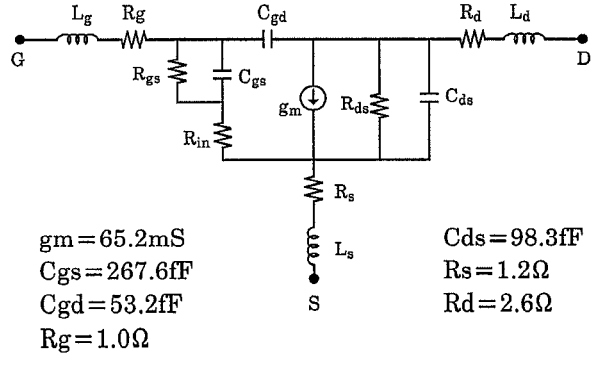

Fig.8 Equivalent circuit of 0.3 μm FET. (Vds=2.0V, Id=0.2Idss)

Noise-figure measurements were performed on device using an HP-8970B noise figure meter. The noise figures and associated gains versus bias current at 12GHz and 18GHz are shown in Fig.9. Minimum noise figures of 0.72dB (1.15dB) with associated gains of 10.5dB (8.5dB) were measured at 12 GHz (18GHz).

In addition,optimized noise figures are very insensitive to the bias current. Those characteristics give a large design margin for bias conditions in low noise amplifier ICs. The frequency dependence of minimum noise figure is shown in Fig.10. According to the Fukui noise equation [11],

$Fmin = 1 + Kf(f/f_T)\{gm(Rs + Rg)\}^{1/2}$

the Kf factor was calculated to be 1.30 by using the equivalent circuit value shown in Fig.9.
These results are comparable to those of AlGaAs/GaAs HEMTs with a same geometry.

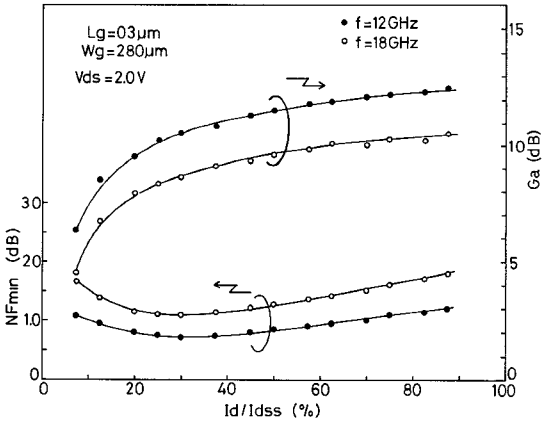

Fig.9 Minimum noise figure (NF_{min}) and associated gain (Ga) as function of drain current at 12GHz and 18GHz.

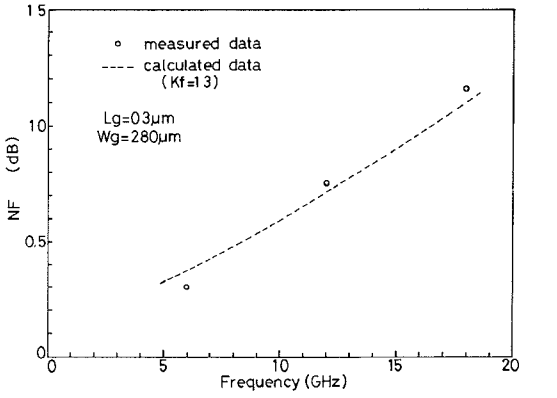

Fig.10 Minimum noise figure versus frequency for a 0.3μm FET. Dashed line shows the calculated results from Fukui noise equation.

Conclusion

We have developed novel pulse-doped GaAs MESFETs. These devices show excellent noise performance comparable to that of AlGaAs/GaAs HEMTs. Furthermore, excellent uniformity and reproducible device characteristics also have been realized. These results demonstrate that newly developed MESFETs are quite promising for high performance and high volume MMIC applications.

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